ABSTRACT OF THE DISCLOSURE

A carrier for use in a chip-scale package, including a semiconductor substrate, such as a semiconductor wafer, with a plurality of apertures formed therethrough. The present invention also includes a chip-scale package including the carrier. When the carrier is employed in such a package, a semiconductor device or a wafer including a plurality of semiconductor devices thereon is invertedly aligned with and disposed over the carrier so that bond pads of the semiconductor device or semiconductor devices substantially align with apertures through the semiconductor substrate. The chip-scale package also includes conductive material disposed in each of the apertures of the semiconductor substrate to form vias through the semiconductor substrate. Conductive traces may extend substantially laterally from selected vias. The chip-scale package may also include a contact or conductive bump disposed in communication with each via. An intermediate layer may be disposed between the semiconductor device and the semiconductor substrate. The intermediate layer may secure the semiconductor device to the semiconductor substrate and insulate structures of the semiconductor device. An insulative layer may be disposed on the semiconductor substrate opposite the semiconductor device. If the chip-scale package includes an intermediate layer or an insulative layer, the electrically conductive vias that extend through the semiconductor substrate are preferably exposed through such layers. The present invention also includes methods of fabricating the semiconductor substrate and assembling a chip-scale package of the invention, including substantially simultaneously assembling semiconductor devices and carrier substrates on a wafer-scale and singulating individual chip-scale packages from the assembled wafers.

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